WHAT IS CLAIMED IS:

1. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said bus.

2. The microprocessor system of Claim 1 in which said multiplexing means includes a plurality of latches for providing the row addresses to said dynamic random access memory.

3. A microprocessor system, comprising a central processing unit, a memory, a bus connecting said central processing unit to said memory, and means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

4. The microprocessor system of Claim 3 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item.

5. The microprocessor system of Claim 4 additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to

said second push down stack.

6. The microprocessor system of Claim 5 in which said second push down stack comprises a register file and said means for storing a top item and said register file are bidirectionally connected.

7. The microprocessor system of Claim 3 additionally comprising means connected to said means for fetching multiple instructions for determining if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

8. The microprocessor system of Claim 3 in which said microprocessor system, including said memory, is contained in an integrated circuit, said memory is a dynamic random access memory, and said means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

9. The microprocessor system of Claim 3 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means

for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

10. The microprocessor system of Claim 9 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions.

11. The microprocessor system of Claim 3 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing a variable width operand, and means connected to said counter to select the variable width operand in response to said counter.

12. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic

random access memory, a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory.

13. A microprocessor system, comprising a central processing unit, a direct memory access processing unit, a memory, a bus connecting said central processing unit and said direct memory access processing unit to said memory, said memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

14. A microprocessor system comprising an arithmetic logic unit, a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, a register file, said means for storing a top item being connected to provide an input to said register file.

15. The microprocessor system of Claim 14 in which said register file comprises a second push down stack and said means for storing a top item and said register file are bidirectionally connected.

16. A data processing system, comprising a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between said memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

17. The data processing system of Claim 16 in which the predetermined electrical level is a predetermined voltage.

18. The data processing system of Claim 17 in which said memory is a dynamic random access memory.

19. A microprocessor system, comprising a central processing unit and a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

20. The microprocessor system of Claim 19 additionally comprising an input/output interface connected to exchange coupling control signals, addresses and data with said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

21. The microprocessor system of Claim 20 in which said second clock is a fixed frequency clock.

22. A microprocessor system, comprising a central

processing unit, a memory, a bus connecting said central processing unit to said memory, said central processing unit including an arithmetic logic unit and a push down stack connected to said arithmetic logic unit, said push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, said push down stack having a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

23. The microprocessor system of Claim 22 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

24. A microprocessor system, comprising a central processing unit, said central processing unit including an arithmetic logic unit, a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO", until said down counter completes a count, the polynomial to be generated resulting in said first register.

25. A microprocessor system, comprising a central processing unit, said central processing unit including an arithmetic logic unit, a result register connected to supply a first input to said arithmetic logic unit, a first, left shifting shifter connected between an output of said arithmetic logic unit and said result register, a multiplier register connected to receive a multiplier in bit reversed form, an output of said multiplier register being connected to a second, right shifting shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply a multiplicand to said arithmetic

logic unit, a down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a multiply instruction to add the contents of said result register with the contents of said third register when the least significant bit of said multiplier register is a "ONE" and to pass the contents of said result register unaltered when the least significant bit of said multiplier is a "ZERO", until said down counter completes a count, the product resulting in said first register.

26. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said bus, and

means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

27. The microprocessor system of Claim 26 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item.

28. The microprocessor system of Claim 27

additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack.

29. The microprocessor system of Claim 28 in which said second push down stack comprises a register file and said means for storing a top item and said register file are bidirectionally connected.

30. The microprocessor system of Claim 29 additionally comprising means connected to said means for fetching multiple instructions for determining if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

31. The microprocessor system of Claim 30 in which said microprocessor system, including said memory, is contained in an integrated circuit, said memory is a dynamic random access memory, and said means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

32. The microprocessor system of Claim 30 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being

connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

33. The microprocessor system of Claim 32 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions.

34. The microprocessor system of Claim 33 in which said means for decoding is configured to control said counter in response to an instruction utilizing a variable width operand, said microprocessor system additionally comprising means connected to said counter to select the variable width operand in response to said counter.

35. The microprocessor system of Claim 34 additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory.

36. The microprocessor system of Claim 35 additionally comprising a direct memory access processing unit, said bus connecting said direct memory access

processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

37. The microprocessor system of Claim 36 in which said central processing unit includes an arithmetic logic unit, a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, a register file, said means for storing a top item being connected to provide an input to said register file.

38. The microprocessor system of Claim 37 in which said register file comprises a second push down stack and said means for storing a top item and said register file are bidirectionally connected.

39. The microprocessor system of Claim 38 in which said microprocessor system includes a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

40. The microprocessor system of Claim 39 in which the predetermined electrical level is a predetermined voltage.

41. The microprocessor system of Claim 40 additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

42. The microprocessor system of Claim 41 additionally comprising an input/output interface connected to exchange coupling control signals, addresses and data with said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

43. The microprocessor system of Claim 42 in which said second clock is a fixed frequency clock.

44. The microprocessor system of Claim 43 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

45. The microprocessor system of Claim 44 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack

elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

46. The microprocessor system of Claim 45 additionally comprising a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO", until said down counter completes a count, the polynomial to be generated resulting in said first register.

47. The microprocessor system of Claim 46 in which said first register is a result register, said first shifter is a left shifting shifter, said second register is a multiplier register connected to receive a multiplier in bit reversed form, said second shifter is a right shifting shifter, said third register is connected to supply a multiplicand to said arithmetic logic unit, said down counter is configured for counting down a number corresponding to one less than the number of digits of the multiplier, said arithmetic logic unit being responsive to a multiply instruction to add the contents of said result register with the contents of said third register, if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO" until said down counter completes a count, the product resulting in said first register.

48. A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program

counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

49. The microprocessor of Claim 48 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

50. The microprocessor of Claim 48 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

51. The microprocessor of Claim 50 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

52. The microprocessor of Claim 50 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuitand said means for fetching instructions includes a column latch for

receiving the multiple instructions.

53. The microprocessor of Claim 48 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

54. The microprocessor of Claim 48 additionally comprising a ring counter variable speed system clock connected to said main central processing unit, said main central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

55. The microprocessor of Claim 54 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

56. The microprocessor of Claim 48 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to

said single integrated circuit.

57. The microprocessor of Claim 56 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

58. In a microprocessor system, a method for fetching instructions, each having a first plurality of bits, from a memory, which comprises providing an instruction register having a second plurality of bits constituting a multiple of the first plurality of bits, fetching a first set of multiple sequential instructions in a single memory cycle, storing the multiple sequential instructions in the instruction register, determining if the multiple instructions require a memory access, and fetching a second set of multiple instructions during execution of the first set of multiple instructions if the first set of multiple instructions do not require access to the memory.

59. The method of Claim 58 in which a portion of the multiple sequential instructions are skipped in response

to a SKIP instruction.

60. The method of Claim 58 in which a portion of the multiple sequential instructions are repeated a predetermined number of times in response to a MICROLOOP instruction.

61. The method of Claim 58 additionally comprising the steps of storing an instruction utilizing a variable width operand and the variable width operand in said instruction register, determining if the instruction utilizes a variable width operand, and selecting the width of the operand for output from said instruction register in response to the instruction using the variable width operand.

62. The method of Claim 58 additionally comprising the steps of storing a plurality of instructions in a read only memory, fetching selected instructions from the plurality of instructions, assembling the multiple sequential instructions, and storing the multiple sequential instructions in a random access memory prior to fetching the multiple sequential instructions.

63. In a microprocessor connected to a memory by an output enable line, a method for determining when an enable signal can be sent to said memory, which comprises sensing a predetermined electrical level on said output enable line, and providing the enabling signal on said output line in response to the predetermined electrical level.

64. The method of Claim 63 in which the predetermined electrical level is a voltage.

65. In a microprocessor integrated circuit, a method

for clocking the microprocessor, which comprises fabricating a ring counter system clock and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication, and using the ring counter system clock for clocking the microprocessor.

66. The method of Claim 65 additionally comprising the steps of providing an input/output interface for the microprocessor integrated circuit and clocking the input/output interface with a second clock independent of the ring counter system clock.

67. The method of Claim 66 in which the second clock is a fixed frequency clock.

68. In a microprocessor system, a method for operating a push down stack, which comprises providing a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, the first and second plurality of stack elements being provided in a single integrated circuit with the microprocessor, providing a third plurality of stack elements configured as a random access memory external to the single integrated circuit, storing items in the push down stack, popping up to a first plurality of items from the first plurality of stack elements without accessing the second plurality of stack elements, popping a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty, popping up to the second plurality of items from the second plurality of stack elements without accessing the third plurality of stack elements, and popping a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty.

69. A method for generating a polynomial, which comprises providing a starting polynomial value, right shifting feedback terms for the polynomial, determining if a least significant bit of the starting polynomial value is a "ONE" or a "ZERO", performing an exclusive OR of the shifted feedback terms for the polynomial with the feedback terms for the polynomial if the least significant bit of the starting polynomial is a "ONE", right shifting the shifted feedback terms for the polynomial if the least significant bit of the the starting polynomial is a "ZERO", and repeating the above operations a total number of times equal to the number of digits of the polynomial to be generated.

70. A method of multiplying, which comprises providing a multiplier, a multiplicand and a "ZERO", determining if a least significant bit of the multiplier is a "ONE" or a "ZERO", adding the multiplicand and the "ZERO" and shifting the sum left if the least significant bit of the multiplicand is a "ONE", storing the "ZERO" if the least significant bit of the the starting polynomial is a "ZERO", to give a partial result, shifting the multiplier right to give a right shifted multiplier, and repeating the above operations, using the right shifted multiplier in place of the multiplier and the partial result in place of the given "ZERO" after the first time the operations are performed, and shifting the sum of the partial result and the multiplicand or the passed through partial result left to carry out the operations a total number of times equal to one less than the number of digits in the multiplier, to give a desired product.

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